Claims

[c1] 1. A method for processing a semiconductor wafer comprising the steps of:

(a) etching one or more first regions of a wafer according to a first set of etch variables, where a remaining portion of said wafer is prevented from being etched; and

(b) etching one or more other regions of said remaining portion of said wafer according to another set of etch variables, wherein one or more previously etched first regions and any remaining portion of said wafer is prevented from being etched.

[c2] 2. The method of Claim 1 wherein step b) is performed N times for etching N regions of said any remaining portion of said wafer, where N is a whole number equal to or greater than 1.

[c3] 3. The method of Claim 1 where said first set of etch variables and said another set of etch variables include etch chemistry, etch time, tool chuck temperature, tool wall temperature, plasma power, etch concentration, etch bias, and gas ratio.

[c4] 4. The method of Claim 2 where step a) further comprises:

depositing a first layer of photoresist atop said wafer;

patterning aid first layer of photoresist to expose said one or more first regions of said wafer, where said remaining portion

of said wafer is protected by a first patterned photoresist;

etching said wafer where one or more exposed portions of said wafer is etched while a first patterned photoresist protects said remaining portion of said wafer from etch; and

stripping aid first patterned photoresist.

[c5] 5. The method of Claim 2 where step b) further comprises depositing secondary layer of photoresist atop said wafer;

patterning aisd secondary layer of photoresist where said one or more other regions of said wafer is exposed and where said one or more previously etched regions and said any remaining portion of said wafer are protected by a second patterned resist;

etching said wafer where said one or more other regions of said wafer is etched while said second patterned resist protects said one or more previously etched regions and said any remaining portion of said wafer from being further etched; and

stripping said second patterned photoresist.

[c6] 6. The method of Claim 4 where step b) further comprises depositing a secondary layer photoresist atop said wafer;

patterning said secondary layer of photoresist where said one or more other regions of said wafer is exposed and where said one or more previously etched regions and said any remaining portion of said wafer are protected by a second patterned

resist;

etching said wafer where said one or more other regions of said wafer is etched while said second patterned resist protects said one or more previously etched regions and said any remaining portion of said wafer from being further etched; and

stripping said second patterned photoresist.

[c7] 7. The method of Claim 6 where step a) further comprises:
measuring one or more first etched regions; and
comparing said one or more first etched regions to a predetermined specification.

[c8] 8. The method of Claim 6 where step b) further comprises:
measuring one or more other etched regions; and
comparing said one or more other etched regions to another predetermined specification.

[c9] 9. The method of Claim 6 where said patterning further comprises transferring an image to a light sensitive layer of photoresist where said image is produced by a recticle having an opaque region, where said light image determines said one or more first regions and said one or more other regions.

[c10] 10. The method of Claim 6 where said patterning further includes utilizing one or more reticle blinders to direct light to said one or more first regions and said one or more other

regions.

[c11] 11. The method of Claim 6 where said one or more first regions of said wafer are processed for a first chip design and where said one or more other regions of said wafer are processed for a second chip design.

[c12] 12. The method of Claim 6 where said first photoresist pattern and said second photoresist pattern form an etch matrix.

[c13] 13. The method of Claim 6 where said first photoresist pattern is a first line stripe of photoresist across said wafer having a first line stripe width.

[c14] 14. The method of Claim 13 where said line stripe of photoresist is etched to decrease said first line stripe width.

[c15] 15. The method of Claim 14 where said second photoresist pattern is one or more other line stripes of photoresist across said wafer having one or more other line strip widths, where said one or more other line stripe widths are narrower than said first line stripe width of photoresist.

[c16] 16. The method of Claim 15 where said one or more other line stripes of photoresist is etched to decrease one or more other line stripe widths.

[c17] 17. The method of Claim 6 where said wafer comprises at least one material layer atop substrate, where said at least

one material layer includes alumina, poly-Si, silicon, TiN, TaN, oxide, nitride, polyimide or combinations thereof.

[c18] 18. The method of Claim 6 further comprising reworking said first layer of photoresist prior to depositing a secondary layer of photoresist.

[c19] 19. A method for processing a semiconductor wafer comprising the steps of

a) doping at least one first region of a wafer with a first set of doping variables, where a remaining portion of said wafer is prevented from being doped; and

b) doping one or more other regions of said remaining portion of said wafer according to another set of doping variables, wherein one or more previously doped first regions and any remaining portion of said wafer is prevented from being doped.

[c20] 20. The method of Claim 19, where said first set of doping variables and said another set of doping variables comprise dopant species, dopant concentration, and implant energy.